REMARKS

Claims 20 and 28-56 are pending in this application, with claims 20, 34, 41 and 49 being independent. Claims 20, 34, 41 and 49 have been amended. In particular, claims 20, 34, 41 and 49 have been amended to recite that the side recessed portions are "formed by overetching." Support for this amendment may be found in the application at least on page 4, lines 1-3. Claims 34 and 49 have been further amended to recite "a wiring." Support for this amendment may be found in the application at least on page 10, lines 24-30 and in Fig. 3C. Fig. 3C of the application has also been amended. Specifically, Fig. 3C has been amended to include an additional reference numeral "320" to clearly denote that the same mixed layer 320 is in contact with both the semiconductor layer region 209 and the gate electrode 208. The amendment to Fig. 3C is included only for clarity and is fully supported by the cross-hatching of layer 320 in Fig. 3C as originally filed. No new matter has been added.

Claims 34-40 and 49-56 have been rejected as failing to comply with the written description requirement. In particular, the Examiner asserts that the specification does not provide support for a first side recessed portion and a second side recessed portion (i.e., two separate regions) being filled with one layer. Applicants traverse this rejection and refer the Examiner to Fig. 3C, which shows the same layer 320 as filling both a first side recessed portion formed by overetching to contact the semiconductor layer region 209 and a second side recessed portion formed by overetching to contact the gate electrode 208. Applicants have amended Fig. 3C to more clearly indicate this.

Claims 34-56 have been rejected as being indefinite. Specifically, the Examiner asserts that it is unclear which electrode is being referenced in the claimed limitation "the electrode contains a first layer and a second layer." Applicants have amended independent claims 34 and 49 for clarity. As amended, the electrode being referenced in the cited limitation is "the electrode" and not "the gate electrode." Applicants, therefore, request reconsideration and withdrawal of this rejection.

Independent claims 20 and 41, and their dependent claims 28, 31, 32, 42 and 45-47, have been rejected as being anticipated by Takafuji (U.S. Patent No. 4,746,628). Each of independent

claims 20 and 41, as amended, recites "a semiconductor layer on an insulating surface, wherein the semiconductor layer has a side recessed portion formed by overetching" (emphasis added). Applicants request reconsideration and withdrawal of the rejection of claims 20 and 41, and their dependent claims, because Takafuji does not describe or suggest the recited semiconductor layer having a side recessed portion formed by overetching.

In Takafuji, the low resistance area 70, which the Examiner equates to the recited side recessed portion, of the silicon layer 40 is not formed by overetching, as claimed. Rather, it is formed through deposition. See col. 3, lines 7-11.

For at least these reasons, applicants request reconsideration and withdrawal of the rejection of claims 20 and 41, and their dependent claims 28, 31, 32, 42 and 45-47.

Claims 29, 30, 43 and 44, which depend from claims 20 and 41, have been rejected as being unpatentable over Takafuji in view of Zhang (U.S. Patent No. 5,313,075). Claims 33 and 48, which also depend from claims 20 and 41, have been rejected as being unpatentable over Takafuji in view of Applicant Admitted Prior Art (AAPA). Neither Zhang, AAPA, nor any proper combination of the two remedies the failure of Takafuji to describe or suggest the recited semiconductor layer having a side recessed portion formed by overetching, as recited in claims 20 and 41. Accordingly, applicants request reconsideration and withdrawal of the rejection of claims 29, 30, 33, 43, 44 and 48.

Independent claims 34 and 49, and their dependent claims 35, 38, 39, 50 and 53-55, have been rejected as being unpatentable over Takafuji in view of Davies (U.S. Patent No. 5,712,501). Each of independent claims 34 and 49 recites "a semiconductor layer on an insulating surface, wherein the semiconductor layer has a first side recessed portion formed by overetching", "a gate electrode ... wherein the gate electrode has a second side recessed portion formed by overetching" and "a wiring ... wherein ... the wiring contains a first layer and a second layer." Applicants requests reconsideration and withdrawal of the rejection of claims 34 and 49, and their dependent claims, because neither Takafuji, Davies, nor any proper combination of the two describes or suggests (1) the recited semiconductor layer having a first side recessed portion

formed by overetching; (2) the recited gate electrode having a second side recessed portion formed by overetching; and (3) the recited wiring containing a first layer and a second layer.

As described above, Takafuji does not describe or suggest the recited semiconductor layer having a first side recessed portion formed by overetching. Davies does not remedy the failure of Takafuji to describe or suggest this feature. Specifically, Davies does not describe or suggest that the portion of the source region 13 that receives the source electrode 21, which the Examiner equates to the recited first side recessed portion, is formed by overetching, as claimed. Rather, this portion and the source electrode 21 are formed through a silicide process. See col. 6, lines 24-26.

Moreover, as acknowledged by the Examiner, Takafuji does not describe or suggest a gate electrode having a second side recessed portion, and, therefore, does not describe or suggest the recited gate electrode having a second side recessed portion formed by overetching. See page 5 of Office Action. Davies does not remedy the failure of Takafuji to describe or suggest this feature. In Davies, the portion of the semiconductor material 23 that receives the gate electrode 26, which the Examiner equates to the recited second side recessed portion, is not formed by overetching, as claimed. Rather, this portion and the gate electrode 26 are formed through a silicide process. See col. 6, lines 24-26.

Finally, Takafuji and Davies do not describe or suggest the recited wiring formed of a first layer and a second layer. In particular, Takafuji does not describe or suggest a wiring formed of low resistance area 70, which the Examiner equates to the recited first layer, and source electrode 50, which the Examiner equates to the recited second layer. Similarly, Davies does not describe or suggest a wiring formed of the source electrode 21 and the gate electrode 26, which the Examiner equates to the recited first layer, and an additional layer.

For at least these reasons, applicants request reconsideration and withdrawal of the rejection of claims 34 and 49, and their dependent claims 35, 38, 39, 50 and 53-55.

Claims 36, 37, 51 and 52, which depend from claims 34 and 49, have been rejected as being unpatentable over Takafuji in view of Davies and Zhang. Claims 40 and 56, which also depend from claims 34 and 49, have been rejected as being unpatentable over Takafuji in view of

Davies and AAPA. Neither Zhang, AAPA, nor any proper combination of the two remedies the failure of Takafuji and Davies to describe or suggest the features of the independent claims discussed above. Accordingly, applicants request reconsideration and withdrawal of the rejection of claims 36, 37, 40, 51, 52 and 56.

Applicants submit that all claims are in condition for allowance.

No fees are believed due. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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